REMARKS

Claims 13-14, 16-17, and 25-40 are currently pending. Claims 13, 16, 25, 33, 35 and 38 have been amended. No new matter has been added with this amendment.

In view of the present remarks and previous amendments, Applicant submits that claims 13-14, 16-17 and 25-40 are in condition for allowance as each claim recites the use of flash memory and the displaying of the operational status representative of flash memory parameters such as number of write operations, error frequency and remaining useful life of this flash memory.

To review the arguments previously submitted, Applicant summarizes as below:

1. Yamagami et al. is directed towards flash memory but does not describe a display means.

2. Yoshito is directed towards traditional bit memory which is an art completely different from the flash memory of Yamagami and, therefore, should not be combined with Yamagami.

3. Yoshito pertains to display of raw bit storage capacity while the present invention displays an operational status of the flash memory and does not provide a display of remaining available operations, e.g., read, write, error frequency.

Response to Arguments

In the Final Office Action dated February 9, 2005, it was asserted that Yamagami et al. and Yoshito are analogous arts because IC memory design is taught. This statement casts an overly broad net regarding what can be considered as analogous art with respect to the electronic

arts, i.e., virtually anything that includes an electronic component. Further, this statement is contrary to Federal Circuit precedent.

In *Wang Laboratories v. Toshiba Corp.* (26 USPQD 2d 1767, (Fed. Cir. 1993)), the Federal Circuit determined that prior art teaching the use of Static Random-Access-Memories (SRAM's) did not suggest the use of Dynamic Random-Access-Memories (DRAM's). More to the point, Judge Lourie explicitly stated that, "The Allen-Bradley art is not the same field of endeavor as the claimed subject matter merely because it relates to memories." *Wang* at 1773. (Emphasis added.)

Two criteria are relevant in determining whether prior art is analogous. First, the art must be from the same field of endeavor, regardless of the problem addressed. Second, if the art is not from the same field of endeavor, it must be reasonably pertinent to the particular problem to be solved.

With respect to the first criteria, the flash memory addressed by Yamagami et al. and the traditional bit memory addressed by Yoshito are not from the same field of endeavor in much the same way as the SRAM and DRAM of *Wang* were determined to be not in the same field of endeavor. Flash memory and traditional bit memory reflect different endeavors in that their structure and use are completely different.

With respect to the second criteria, Yoshito's display of remaining raw bit storage capacity is not at all pertinent to the flash memory problems addressed by the present claims. As discussed in previous responses, the display as presently claimed relates to **operational capacity** of the flash memory relating to the finite number of write/rewrite operations a flash memory unit is capable of before failing. Displaying the remaining life of the flash memory is not at all

pertinent to a display of remaining storage capacity for bit memory as bit memory does not suffer the write/rewrite limitations of flash memory.

For the above reasons, the Yamagami et al. and Yoshito are not analogous and as such, they should not be combined to reach a conclusion of obviousness.

Claim Rejections – 35 U.S.C. § 103

In the Office Action of February 9, 2005, claims 13-14, 16-17 and 25-40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamagami et al. in view of Yoshito et al. and in further view of U.S. Patent No. 6,112,984 to Snavely. As discussed above, Yamagami et al. and Yoshito et al. are nonanalogous art and are not combinable to reach a conclusion of obviousness. Snavely includes references to flash memory but fails to render Yamagami et al. and Yoshito et al. as being analogous art.

With respect to the combination of Yamagami et al. and Snavely, which both address flash memory, Applicant has amended independent claims 13, 16, 25, 33, 35 and 38 to further clarify and make explicit that the problem cured by the amended claims is related to the display of the operational status of the flash memory based on various flash memory parameters such as number of write operations, error frequency and remaining useful life. As noted in the Final Office Action, Yamagami et al. fails to describe the claimed display. Snavely does describe flash memory 121 as containing messages to display on LCD 91. However, these messages are for the operational status of an electrical wallet as opposed to an operational status of the flash memory as presently claimed. As described at Col. 6, Line 33 – Page 7, Line 10, LCD 91 can display messages from flash memory 121 relating to financial account information, personal information data, encryption codes, updated account and phone numbers. None of the

information displayed by LCD 91 is at all relevant nor does it disclose the display of information representative of the operational status of the flash memory as presently claimed.

Prima facie obviousness is not established if all the elements of the rejected claim are not disclosed or suggested in the cited art. *In re Ochiai*, 37 USPQ 1127, 1131 (Fed. Cir. 1995). ("The test for obviousness *vel non* is statutory. It requires that one compare the claims' 'subject matter as a whole' with the prior art 'to which said subject matter pertains.'"). See also, MPEP 2143.03 "All Claim Limitations Must Be Taught or Suggested," citing *In re Royka*, 180 USPQ 580 (CCPA 1974). "To establish *prima facie* obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art." MPEP 2143.03. Because Yamagami et al. and Snavely **fail to disclose, suggest or teach** ***all*** of the limitations of presently amended independent claims 13, 16, 25, 33, 35 and 38, either individually or in combination, Applicant respectfully submits that a *prima facie* case of obviousness has not been established and an Official Action acknowledging same is respectfully requested.

Claim Rejections – 35 U.S.C. § 102

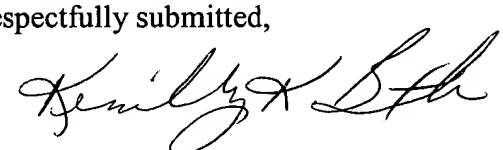
In the Final Office Action of February 9, 2005, claims 13-14, 16-17 and 25-40 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,222,109 to Pricer.

"For a prior art reference to anticipate in terms of 35 U.S.C. § 102, **every element of the claimed invention must be identically shown in a single reference**. These elements must be arranged as in the claim under review, but this is not an 'ipsissimis verbis' test." *In re Bond*, 15 USPQ2d 1566, 1567 (Fed. Cir, 1990)(Internal citations omitted and emphasis added.). Pending claims 13-14, 16-17 and 25-40 all include a limitation directed to a display element. Pricer fails to disclose such a display element. Because Pricer fails to disclose all of the limitations of

pending claims 13-14, 16-17 and 25-40, Applicant respectfully submits that the burden necessary to establish a *prima facie* case of anticipation has not been met and an Official Action acknowledging same is respectfully requested.

In view of the foregoing, it is submitted that this application is in condition for allowance. Favorable consideration and prompt allowance of the application are respectfully requested. The Examiner is invited to telephone the undersigned if the Examiner believes it would be useful to advance prosecution.

Respectfully submitted,



Kimberly K. Baxter
Registration No. 40,504

Customer No. 24113
Patterson, Thuente, Skaar & Christensen, P.A.
4800 IDS Center
80 South 8th Street
Minneapolis, Minnesota 55402-2100
Telephone: (612) 349-5750